



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,831	09/30/2003	Jimmie Earl DeWitt JR.	AUS920030479US1	6642
35525	7590	12/17/2009		
IBM CORP (YA)				
C/O YEE & ASSOCIATES PC				
P.O. BOX 802333				
DALLAS, TX 75380				
EXAMINER				
GIBOUX, GEORGE				
ART UNIT		PAPER NUMBER		
2183				
NOTIFICATION DATE		DELIVERY MODE		
12/17/2009		ELECTRONIC		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ptonotifs@yeciipaw.com

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

---

*Ex parte* JIMMIE EARL DEWITT JR., FRANK ELIOT LEVINE,  
ENIO MANUAL PINEDA, CHRISTOPHER MICHAEL RICHARDSON,  
and ROBERT JOHN URQUHART

---

Appeal 2008-005166  
Application 10/675,831  
Technology Center 2100

---

Decided: December 15, 2009

---

*Before* LEE E. BARRETT, THU A. DANG, and DEBRA K. STEPHENS,  
*Administrative Patent Judges.*

STEPHENS, *Administrative Patent Judge.*

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134(a) (2002) from a final rejection of claims 1-25. We have jurisdiction under 35 U.S.C. § 6(b) (2008).

We AFFIRM.

### *Introduction*

According to Appellants, the invention is a system and method for obtaining performance data in a data processing system (Spec. 2, BACKGROUND OF THE INVENTION, §1. Technical Field).

## STATEMENT OF THE CASE

### *Exemplary Claim(s)*

Claims 1 and 21 are exemplary claims and are reproduced below:

1. A method in a data processing system for processing instructions, the method comprising:  
responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether a performance indicator that identifies that execution of the instruction is to be monitored is present; and  
forcing an interrupt if the performance indicator is present.

21. A computer program product in a computer readable medium for processing instructions, the computer program product comprising:  
first instructions for responding to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether a performance indicator that identifies that execution of the instruction is to be monitored is present; and  
second instructions for forcing an interrupt if the performance indicator is present.

*Prior Art*

Heisch

US 5,774,724

Jun. 30, 1998

KENNETH L. SHORT, EMBEDDED MICROPROCESSOR SYSTEMS DESIGN:  
AN INTRODUCTION USING THE INTEL 80C188EB (Prentice Hall 1998)  
(hereinafter “Short”).

*Rejections*

Claims 21-25 stand rejected under 35 U.S.C. § 101 as being directed to non-statutory matter.

Claims 1-25 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Heisch.

Claims 1, 6, and 7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Short and Heisch.

GROUPING OF CLAIMS

(1) Appellants argue claims 21-25 as a group (App. Br. 16-18, §C). We therefore treat claims 21-25 as standing or falling with representative claim 21.

(2) Appellants argue claims 1-5, 14-17, and 21-23 as a group based on arguments set forth for claim 1 (App. Br. 10-13, §A.1). We therefore treat claims 2-5, 14-17, and 21-23 as standing or falling with representative claim 1.

(3) Appellants argue claims 8-13, 18-20, and 24-25 as a group based on arguments set forth for claim 8 (App. Br. 13-14, §A.2). We therefore treat claims 9-13, 18-20, and 24-25 as standing or falling with representative claim 8.

(4) Appellants argue claims 1, 6, and 7 as a group based on arguments set forth for claim 1 (App. Br. 14-16, §B). We therefore treat claims 1, 6, and 7 as standing or falling with representative claim 1.

We accept Appellants' grouping of the claims. *See* 37 C.F.R. § 41.37(c)(1)(vii) ("Notwithstanding any other provision of this paragraph, the failure of appellant to separately argue claims which appellant has grouped together shall constitute a waiver of any argument that the Board must consider the patentability of any grouped claim separately.").

## ISSUE 1

### *35 U.S.C. § 101: claims 21-25*

Appellants argue that the Examiner erred in rejecting claims 21-25 under 35 U.S.C. § 101 as no basis exists for holding a computer usable medium claim non-statutory because the medium may be allegedly "intangible" (App. Br. 16, §C). Instead, Appellants argue, the claims recite "clearly functional descriptive material [as] they impart functionality when employed as a computer component" (*id.* at 17, §C). Therefore, "claims 21-25 clearly recited a useful, concrete, and tangible result" (*id.*).

The Examiner disagrees, finding "computer readable media", when read in light of Appellants' Specification, includes transmission-type media (Ans. 15). Therefore, the Examiner concludes the recited inventions are non-statutory (*id.*).

*Issue 1:* Have Appellants shown the Examiner erred in concluding claims 21-25 recite non-statutory material?

## FINDINGS OF FACT (FF)

### *Appellants' Disclosure*

(1) "Examples of computer readable media include recordable-type media, such as a floppy disk, a hard disk drive, a RAM, CD-ROMs, DVD-ROMs, and transmission-type media, such as digital and analog communications links, wired or wireless communications links using transmission forms, such as, for example, radio frequency and light wave transmissions." (Spec. 64).

## PRINCIPLES OF LAW

"The Patent and Trademark Office (PTO) must consider all claim limitations when determining patentability of an invention over the prior art." *In re Lowry*, 32 F.3d 1579, 1582 (Fed. Cir. 1994) (citing *In re Gulack*, 703 F.2d 1381, 1385 (Fed. Cir. 1983)). "Claims must be read in view of the specification, of which they are a part." *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc) (citations omitted).

"A transitory, propagating signal . . . is not a 'process, machine, manufacture, or composition of matter.' Those four categories define the explicit scope and reach of subject matter patentable under 35 U.S.C. § 101." *In re Nuijten*, 500 F.3d 1346, 1357 (Fed. Cir. 2007), *reh'g denied en banc*, 515 F.3d 1361 (Fed. Cir. 2008), *cert. denied*, 129 S.Ct. 70 (2008). "If a claim covers material not found in any of the four statutory categories, that claim falls outside the plainly expressed scope of § 101 even if the subject matter is otherwise new and useful." *Id.* at 1354.

## ANALYSIS

Appellants define computer readable medium as including “transmission-type media” which includes radio frequency and light wave transmissions (FF 1). We find these types of transmissions are transitory and thus, are transitory, propagating signals – a category of subject matter that falls outside the four statutory categories covered within the scope of 35 U.S.C. §101. Accordingly, we conclude Appellants have not shown the Examiner erred in concluding claims 21-25 recite non-statutory material.

## ISSUE 2

*35 U.S.C. § 102(b): claims 1-5, 14-17, and 21-23*

Appellants argue Heisch does not describe “responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether a performance indicator that identifies that execution of the instruction is to be monitored is present” (App. Br. 11, §A.1). Instead, Appellants contend, Heisch describes that the contents of the IAB register are compared to an executing instruction’s address (*id.* at 11-12, §A.1). Appellants further contend Heisch describes “that cache misses may be counted by the performance monitor ‘if it is desired to count cache misses’” and, thus, Heisch does not describe determining whether the performance indicator is present (*id.* at 12, §A.1). Moreover, Appellants argue Heisch monitors all instructions and any “indicator” would indicate whether an interrupt will occur, not whether the execution of an instruction to be monitored is present (*id.*).

The Examiner finds that, due to the use of the term “identity”, Heisch is simply required to recognize that a match between the IABR register contents and the executing instruction’s address occurred and to raise an interrupt in response (Ans. 13). In response to Appellants’ alternative definition of “identity,” the Examiner finds Heisch describes that the performance monitor may be enabled and disabled on a per instruction basis, thus satisfying this “identity” definition (*id.* at 14).

*Issue 2:* Have Appellants met the burden of showing the Examiner erred in finding Heisch discloses “responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether a performance indicator that identifies that execution of the instruction is to be monitored is present?”

## FINDINGS OF FACT (FF)

### *Heisch's Reference*

(2) A microprocessor performance monitor and instruction address breakpoint facility are combined and interconnected to provide performance monitoring through use of an instruction address breakpoint (Abst.).

(3) The instruction address breakpoint may be set for any effective address in a program that uses an instruction address breakpoint register (IABR) (col. 3, l. 64 - col. 4, l. 2). When an instruction at the address in the IABR is executed, the IABR will cause an instruction address breakpoint exception (col. 4, ll. 2-4). The performance monitor may be enabled and disabled on a per instruction address basis (col. 4, ll. 5-7).



(4) First, a selected address is loaded into the IAB register. The contents of the IAB register are compared to the address of the particular instruction executing at a given time. (Col. 5, ll. 58-65 and Fig. 2, block 64).

(5) When it is determined that a preselected IAB address is equal to the address of the instruction currently to be executed, the microprocessor will break out of execution of the current program, passing execution to an interrupt handler specifically initialized to handle that breakpoint or exception (col. 5, l. 66 - col. 6, l. 6).

(6) “In a typical embodiment, the performance monitor 42 includes counter registers which are interrupt driven.” (Col. 6, ll. 43-44). When start and stop addresses are detected the counters are enabled and disabled, as desired. (Col. 6, ll. 46-47).

## PRINCIPLES OF LAW

### *Claim Construction*

“[D]uring examination proceedings, claims are given their broadest reasonable interpretation consistent with the specification.” *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000) (citations omitted).

“In the absence of an express intent to impart a novel meaning to the claim terms, the words are presumed to take on the ordinary and customary meanings attributed to them by those of ordinary skill in the art.” *Brookhill-Wilk 1, LLC v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1298 (Fed. Cir. 2003) (citation omitted). “[T]he words of a claim ‘are generally given their ordinary and customary meaning.’” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (citations omitted). The “ordinary and customary meaning of a claim term is the meaning that the term would have

to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application.” *Id.* at 1313 (citation omitted).

### ANALYSIS

In analyzing the particular limitation, we give the claims their broadest reasonable interpretation. Appellants have not defined or used the term “performance indicator” in their Specification. We find that to a person of ordinary skill in the art, “performance indicator” would have a general meaning of something that indicates performance. As such, we find that the performance indicator is the positive result of the comparison between the IABR and the address of the particular instruction executing. The result is an indicator of the performance of the comparison.

The “determining” occurs when the IABR is compared to the address of the particular instruction executing at that time. If the performance indicator (the positive result) is present, an interrupt is forced. Accordingly, we find Heisch discloses “responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether a performance indicator that identifies that execution of the instruction is to be monitored is present” as disclosed in representative claim 1.

### ISSUE 3

*35 U.S.C. § 102(b): claims 8-13, 18-20, and 24-25*

Appellants argue that Heisch does not disclose that a performance indicator identifies whether monitoring of an access of data is present (App.

Br. 14). Appellants reiterate their contention that Heisch describes that all instructions are monitored and thus, the determination of whether a performance indicator identifying if data access to be monitored is not present (*id.*).

The Examiner maintains the findings set forth for claim 1 also apply to claim 8; thus, the Examiner finds Heisch discloses this monitoring (Ans. 11-14).

*Issue 3:* Have Appellants met the burden of showing the Examiner erred in finding Heisch discloses “responsive to an access of data, determining whether a performance indicator that identifies that access of the data is to be monitored is present”?

## ANALYSIS

As discussed above with respect to claim 1, the performance indicator is the positive result of the comparison between the IABR and the address of the particular instruction executing. When the microprocessor executes instructions, the determining step occurs (FF 3). The determining step compares the IABR to the address of the particular instruction executing at that time (FF 4). If the performance indicator (the positive result) is present, an interrupt is forced (FF 5). Accordingly, we find Heisch discloses “responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether a performance indicator that identifies that execution of the instruction is to be monitored is present.”

#### ISSUE 4

*35 U.S.C. § 103(a): claims 1, 6, and 7*

Appellants reiterate their contention that Heisch does not disclose “responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether a performance indicator that identifies that execution of the instruction is to be monitored is present” as recited in representative claim 1 (App. Br. 15). Appellants further contend Short does not cure the deficiency of Heisch (*id.*). Specifically, Appellants argue Short describes an “interrupt-type” procedure that checks if the opcode of the instruction indicates the interrupt instruction and, if so, will force an interrupt (*id.*). However, according to Appellants, this does not teach “responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether a performance indicator that identifies that execution of the instruction is to be monitored is present.”

The Examiner finds, as found for claim 1, that Heisch discloses this feature. (Ans. 15).

*Issue 4:* Have Appellants shown the Examiner erred in concluding the combination of Short and Heisch teaches the limitations recited in claims 1, 6, and 7?

#### ANALYSIS

As we discussed above with respect to claim 1, Heisch discloses “responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether a

performance indicator that identifies that execution of the instruction is to be monitored is present.” Appellants have not presented any separate arguments for claim 6 and 7 but instead rely on the arguments presented for claim 1. Accordingly, we find Appellants have not shown the combination of Short and Heisch teaches the limitations recited in claims 1, 6, and 7.

### CONCLUSION

We conclude Appellants have not shown the Examiner erred in concluding claims 21-25 recite non-statutory material.

Additionally, we conclude Appellants have not shown the Examiner erred in rejecting claims 1-25 under 35 U.S.C. § 102(b) as being anticipated by Heisch.

Appellants have not shown the Examiner erred in finding Heisch discloses “responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether a performance indicator that identifies that execution of the instruction is to be monitored is present”. Accordingly, Appellants have not met the burden of showing the Examiner erred in rejecting representative independent claim 1 under 35 U.S.C. § 102(b) as being anticipated by Heisch. Independent claims 14 and 21 recite commensurate language and thus Appellants have not shown the Examiner erred with respect to these claims. Claims 2-5 which depend from claim 1, claims 15-17 which depend from claim 14, and claims 22 and 23 which depend from claim 21 were not argued separately but instead Appellants rely on the arguments set forth for representative claim 1. Therefore, we conclude Appellants have not shown

the Examiner erred in rejecting claims 1-5, 14-17, and 21-23 under 35 U.S.C. § 102(b) for anticipation by Heisch.

Appellants have not shown the Examiner erred in finding Heisch discloses “responsive to an access of data, determining whether a performance indicator that identifies that access of the data is to be monitored is present.” Accordingly, we conclude Appellants have not met the burden of showing the Examiner erred in rejecting representative independent claim 8 under 35 U.S.C. § 102(b) as being anticipated by Heisch. Independent claims 18 and 24 recite commensurate language and thus Appellants have not shown the Examiner erred with respect to these claims. Claims 9-13 which depend from claim 8, claims 19 and 20 which depend from claim 18, and claim 25 which depends from claim 24 were not argued separately but instead Appellants rely on the arguments set forth for representative claim 8. Therefore, we conclude Appellants have not shown the Examiner erred in rejecting claims 8-13, 18-20, 24, and 25 under 35 U.S.C. § 102(b) as being anticipated by Heisch.

Further, Appellants have not shown the Examiner erred in concluding Heisch, when taken alone or in combination with Short, discloses “responsive to an access of data, determining whether a performance indicator that identifies that access of the data is to be monitored is present” as recited in representative claim 1. Accordingly, we conclude Appellants have not shown the Examiner erred in rejecting claim 1 under 35 U.S.C. § 103(a) as being obvious over Short and Heisch. Claims 6 and 7 depend from claim 1 and were not separately argued. Therefore, we conclude Appellants have not shown the Examiner erred in rejecting claims 1, 6, and 7 under 35 U.S.C. § 103(a) as being obvious over Short and Heisch.

DECISION

The Examiner's rejection of claims 21-25 under 35 U.S.C. § 101 for reciting non-statutory material is affirmed.

The Examiner's rejection of claims 1-25 under 35 U.S.C. § 102(a) as being anticipated by Heisch is affirmed.

The Examiner's rejection of claims 1, 6, and 7 under 35 U.S.C. § 103(a) as being obvious over Short and Heisch is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv) (2009).

AFFIRMED

nhl

IBM CORP (YA)  
C/O YEE & ASSOCIATES PC  
P.O. BOX 802333  
DALLAS TX 75380